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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Question Set-7 Digital Technologies and Microprocessor

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A. Objectives Questions:

1. In boolean algebra, the OR operation is performed by which properties?
   a) Associative properties
   b) Commutative properties
   c) Distributive properties
   d) All of the Mentioned
2. The expression for Absorption law is given by _____
   a) A + AB = A
   b) A + AB = B
   c) AB + AA' = A
   d) A + B = B + A
3. According to boolean law: A + 1 = ?
   a) 1
   b) A
   c) 0
   d) A'
4. DeMorgan's theorem states that _____
   a) (AB)' = A' + B'
   b) (A + B)' = A' * B
   c) A' + B' = A'B'
   d) (AB)' = A' + B
5. The boolean function A + BC is a reduced form of _____
   a) AB + BC
   b) (A + B)(A + C)
   c) A'B + AB'C
   d) (A + C)B
6. When numbers, letters or words are represented by a special group of symbols, this process is called _____
   a) Decoding
   b) Encoding
   c) Digitizing
   d) Inverting

7. The length of the one-byte instruction is
   a) 2 bytes
   b) 1 byte
   c) 3 bytes
   d) 4 bytes
8. Programmable peripheral input-output port is another name for
   a) serial input-output port
   b) parallel input-output port
   c) serial input port
   d) parallel output port
9. Port C of 8255 can function independently as
   a) input port
   b) output port
   c) either input or output ports
   d) both input and output ports
10. All the functions of the ports of 8255 are achieved by programming the bits of an internal register called
    a) data bus control
    b) read logic control
    c) control word register
    d) none of the mentioned

B. Short Answer Types Questions:

1. What is the need for ALE signal in 8085 microprocessor?
2. List the five interrupt pins available in 8085.
3. Differentiate Software and Hardware interrupts
4. What is mean by TRAP interrupt and its significance?
5. What is the need for interfacing?
6. Compare memory mapped I/O and peripheral mapped I/O
7. What is interrupt?.
8. Name the vectored and non vectored interrupt of 8085 system.
9. What is the need for a timing diagram?
10. Define (i) Instruction cycle (ii) Machine cycle

C. Long Answer Types Questions:

1. Mention the total number of registers of 8086 and show the manner in which they are grouped.
2. Draw the timing diagram of OPCODE FETCH machine cycle.
3. Explain the functions of 8085 signals.
4. Design a microprocessor system to interface an 8K × 8 EPROM and 8K × 8 RAM
5. Describe the status register of 8086.

Solutions:

A. Objectives Questions:

1. Answer: d
   Explanation: The expression for Associative property is given by A+(B+C) = (A+B)+C & A*(B*C) = (A*B)*C.
   The expression for Commutative property is given by A+B = B+A & A*B = B*A.
   The expression for Distributive property is given by A+BC=(A+B)(A+C) & A(B+C) = AB+AC.
2. Answer: a
   Explanation: The expression for Absorption Law is given by: A+AB = A.
   Proof: A + AB = A(1+B) = A (Since 1 + B = 1 as per 1's Property).
3. Answer: a
   Explanation: A + 1 = 1, as per 1's Property.
4. Answer: a
   Explanation: The DeMorgan's law states that (AB)' = A' + B' & (A + B)' = A' * B', as per the Dual Property.
5. Answer: b
   Explanation: (A + B)(A + C) = AA + AC + AB + BC = A + AC + AB + BC (By Commutative Property) = A(1 + C + B) + BC = A + BC (1 + B + C =1 By 1's Property).
6. Answer: b
   Explanation: When numbers, letters or words are represented by a special group of symbols, this process is called encoding. Encoding in the sense of fetching the codes or words in a computer. It is done to secure the transmission of information.
7. Answer: b
   Explanation: This format is only one byte long.
8. Answer: b
   Explanation: The parallel input-output port chip 8255 is also known as programmable peripheral input-output port.
9. Answer: c
   Explanation: Port C can function independently either as input or as output ports.
10. Answer: c
    Explanation: By programming the bits of control word register, the operations of the ports are specified.

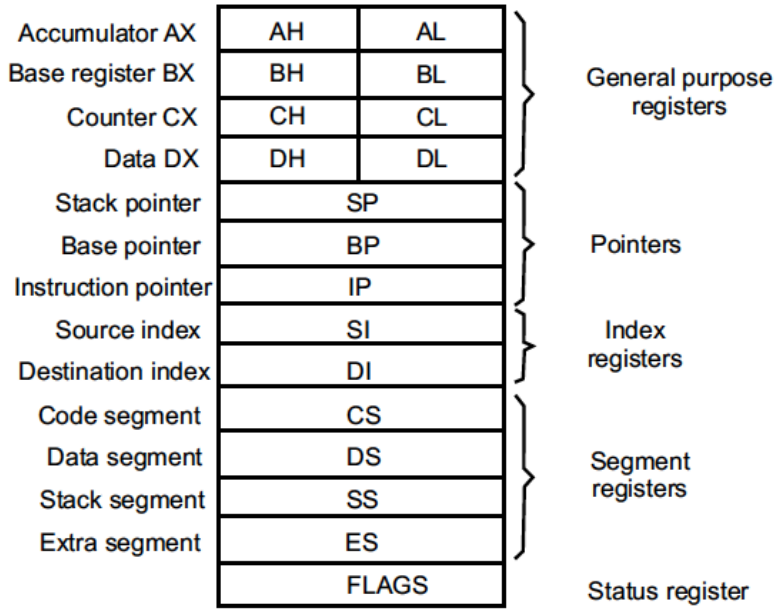
B. Short Answer Types Questions

1. The ALE signal goes high at the beginning of each machine cycle indicating the availability of the address on the address bus, and the signal is used to latch the low order address bus.
2. Interrupt pins are:
   INTR, TRAP, RST 7.5, RST 6.5, RST 5.5
3. The Software interrupt is initiated by the main program, but the hardware interrupt is initiated by the external device. In 8085, Software interrupts cannot be masked or disabled, but in hardware interrupts except TRAP all other interrupts can be masked. In 8086, Software interrupts cannot be masked or disabled, but in hardware interrupts except NMI all other interrupts can be masked.
4. TRAP is a Non maskable interrupt of 8085. It is not disabled by processor reset or after recognition of the interrupt.
5. Generally I/O devices are slow devices. Therefore the speed of I/O devices does not match with the speed of microprocessor. And so an interface is provided between system bus and I/O devices.
6. **Memory Mapped I/O:** 16-bit device address, data transfer between any general-purpose register and I/O port. The memory map (64K) is shared between I/O device and system memory. More hardware is
   required to decode 16-bit address Arithmetic or logic operation can be directly performed with I/O data.
   Peripheral Mapped I/O: 8-bit device address, Data is transfer only between accumulator and I.O port, The I/O map is independent of the memory map; 256 input device and 256. Output device can be connected Less hardware is required to decode 8-bit address, Arithmetic or logical operation cannot be directly performed with I/O data.
7. Interrupt is a signal send by an external device to the processor so as to request the processor to perform a particular task or work
8. When an interrupt is accepted, if the processor control branches to a specific address defined
   by the manufacturer then the interrupt is called vectored interrupt. In Non-vectored interrupt there is no specific address for storing the interrupt service routine. Hence the interrupted device should give the address of the interrupt service routine.
9. The timing diagram provides information regarding the status of various signals, when a machine cycle is executed. The knowledge of timing diagram is essential for system designer to
   select matched peripheral devices like memories, latches, ports, etc, to form a microprocessor system.
10. i) The sequence of operations that a processor has to carry out while executing the
    instruction is called Instruction cycle. Each instruction cycle of a processor indium consists of a number of machine cycles.
    (ii) The processor cycle or machine cycle is the basic operation performed by the processor. To execute an instruction, the processor will run one or more machine cycles in a particular order. Opcode fetch, memory read, memory write, I/O read, I/O write, interrupt acknowledge, halt, hold and reset.

C. Long Answer Types Questions:

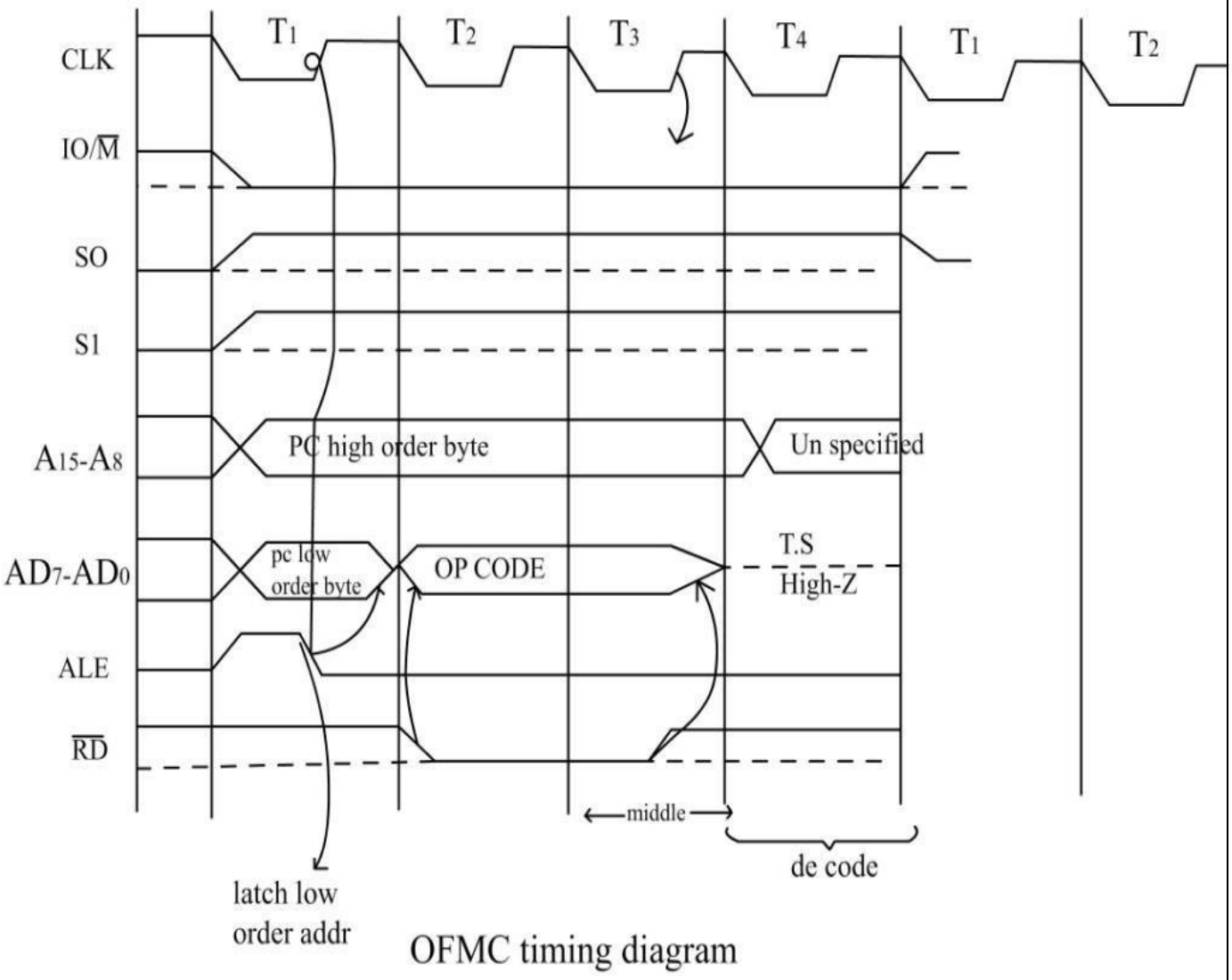
1. .There are in all fourteen numbers of 16-bit registers. The different groups are made as here under:
   - Data group, pointers and index group, status and control flag group and segment group.
   - The data group consists of AX (accumulator), BX (base), CX (count) and DX (data).
   - Pointer and Index group consist of SP (Stack pointer), BP (Base pointer), SI (Source Index), DI (Destination index) and IP (Instruction pointer).
   - Segment group consists of ES (Extra Segment), CS (Code Segment), DS (Data Segment) and SS (Stack Segment).
   - Control flag group consists of a single 16-bit flag register.

Figure below shows the registers placed in the different groups to form a programming model.



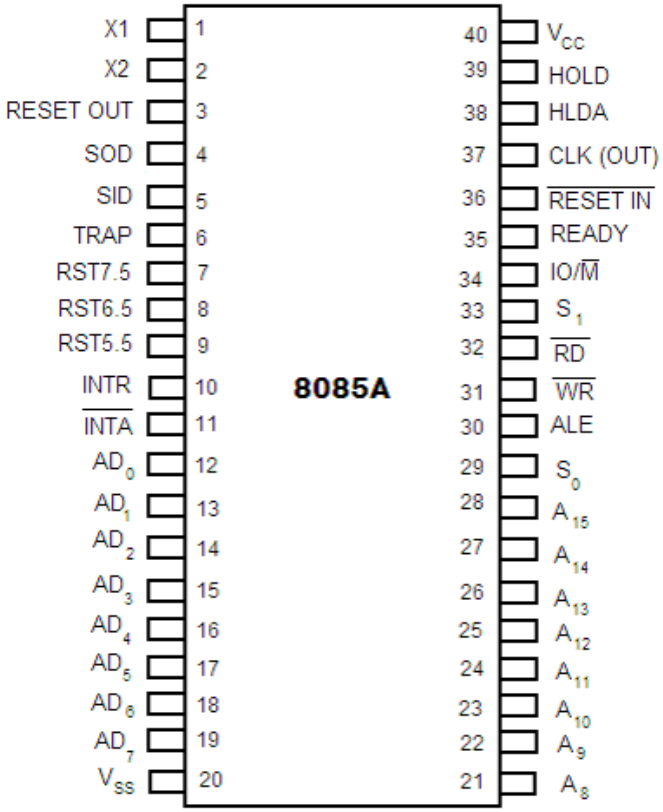
Schematic diagram of intel 8086 registers

2. OPCODE FETCH machine cycle



OFMC timing diagram

3. Pin Diagram and Pin description of 8085



8085 is a 40 pin IC, The signals from the pins can be grouped as follows

- Power supply and clock signals
- Address bus
- Data bus
- Control and status signals
- Interrupts and externally initiated signals
- Serial I/O ports

Power supply and Clock frequency signals:

Vcc: + 5 volt power supply

Vss: Ground

X1, X2 : Crystal or R/C network or LC network connections to set the frequency of internal clock generator. The frequency is internally divided by two. Since the basic operating timing frequency is 3 MHz, a 6 MHz crystal is connected externally. CLK (output)-Clock Output is used as the system clock for peripheral and devices interfaced with the microprocessor.

Address Bus:

A8 - A15: (output; 3-state)

It carries the most significant 8 bits of the memory address or the 8 bits of the I/O address.

Data bus:

AD0 - AD7 (input/output; 3-state)

These multiplexed set of lines used to carry the lower order 8 bit address as well as data bus.

- During the opcode fetch operation, in the first clock cycle, the lines deliver the lower order address A0 - A7. •In the subsequent IO / memory, read / write clock cycle the lines are used as data bus.
- The CPU may read or write out data through these lines.

Control and Status signals:

ALE (output) - Address Latch Enable.

- It is an output signal used to give information of AD0-AD7 contents.
- It is a positive going pulse generated when a new operation is started by uP.
- When pulse goes high it indicates that AD0-AD7 are address.
- When it is low it indicates that the contents are data.

RD (output 3-state, active low)

- Read memory or IO device.
- This indicates that the selected memory location or I/O device is to be read and that the data bus is ready for accepting data from the memory or I/O device

WR (output 3-state, active low)

- Write memory or IO device.
- This indicates that the data on the data bus is to be written into the selected memory location or I/O Devices.

IO/M (output) - Select memory or an IO device.

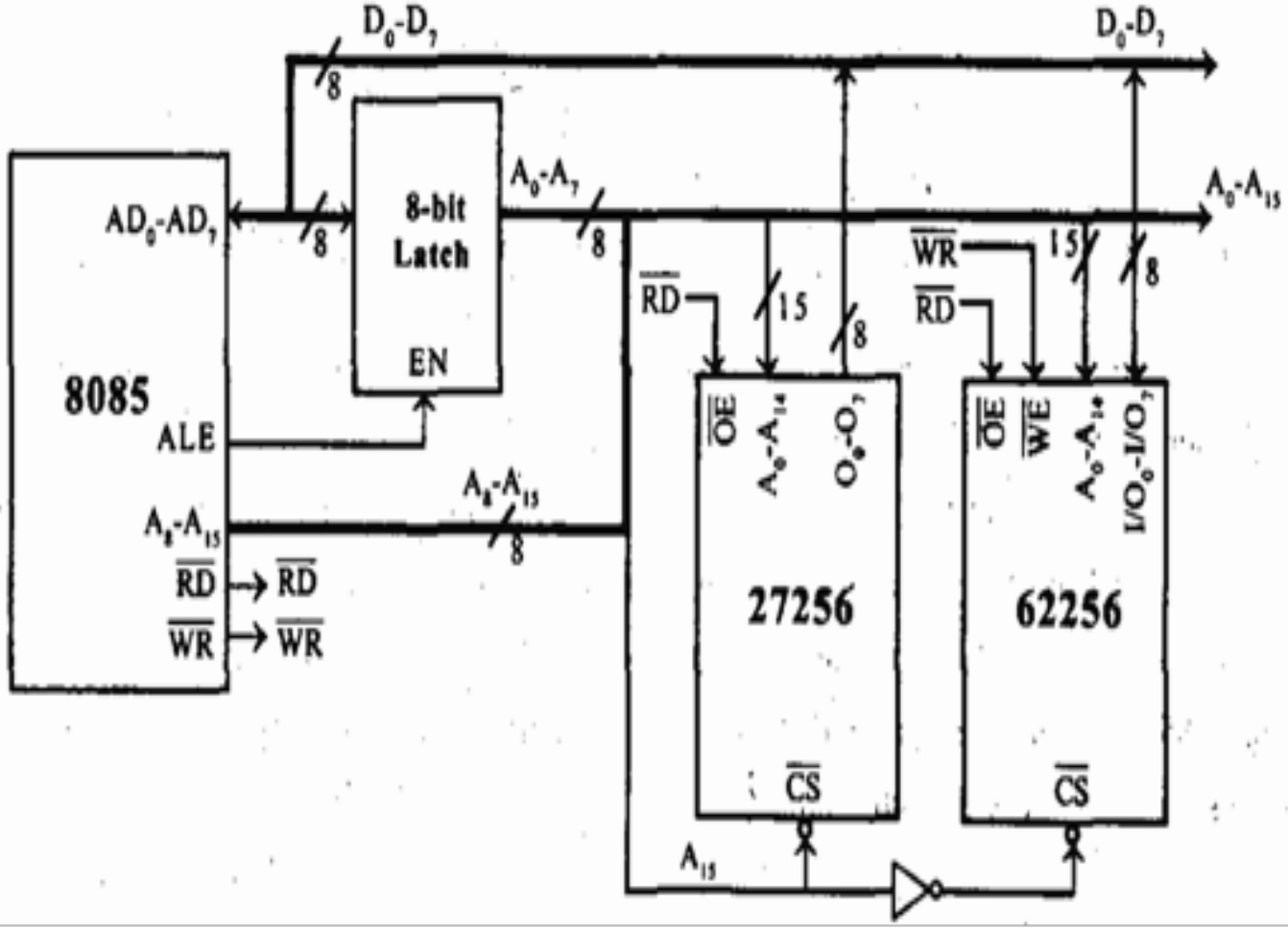
This status signal indicates that the read / write operation relates to whether the memory or I/O device.

It goes high to indicate an I/O operation.

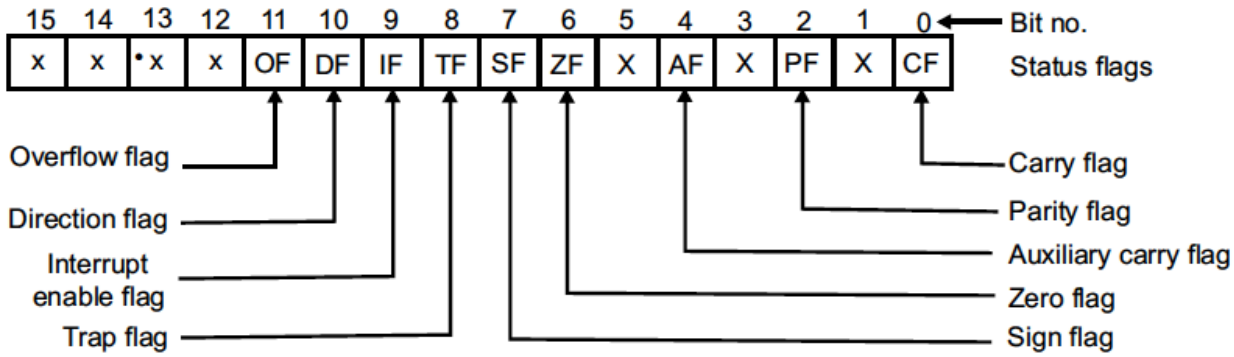
It goes low for memory operations

4. Consider a system in which the available 64kb memory space is equally divided between EPROM and RAM. Interface the EPROM and RAM with 8085 processor.

- Implement 32kb memory capacity of EPROM using single IC 27256.
- 32kb RAM capacity is implemented using single IC 62256.
- The 32kb memory requires 15 address lines and so the address lines A0 - A14 of the processor are connected to 15 address pins of both EPROM and RAM.
- The unused address line A15 is used as to chip select. If A15 is 1, it select RAM and If A15 is 0, it select EPROM.
- Inverter is used for selecting the memory.
- The memory used is both Ram and EPROM, so the low RD and WR pins of processor are connected to low WE and OE pins of memory respectively.
- The address range of EPROM will be 0000H to 7FFFH and that of RAM will be 7FFFH to FFFFH. Two sets of above procedure is used for 64kb of EPROM and RAM.



5. It is a 16-bit register, also called flag register or Program Status Word (PSW). Seven bits remain unused while the rest nine are used to indicate the conditions of flags. The status\flags of the register are shown below in Figure below.



Status flags of intel 8086

Out of nine flags, six are condition flags and three are control flags. The control flags are TF (Trap), IF (Interrupt) and DF (Direction) flags, which can be set/reset by the programmer, while the condition flags [OF (Overflow), SF (Sign), ZF (Zero), AF (Auxiliary Carry), PF (Parity) and CF (Carry)] are set/reset depending on the results of some arithmetic or logical operations during program execution. CF is set if there is a carry out of the MSB position resulting from an addition operation or if a borrow is needed out of the MSB position during subtraction. PF is set if the lower 8-bits of the result of an operation contains an even number of 1's. AF is set if there is a carry out of bit 3 resulting from an addition operation or a borrow required from bit 4 into bit 3 during subtraction operation. ZF is set if the result of an arithmetic or logical operation is zero. SF is set if the MSB of the result of an operation is 1. SF is used with unsigned numbers. OF is used only for signed arithmetic operation and is set if the result is too large to be fitted in the number of bits available to accommodate it. The functions of the flags along with their bit positions are shown below.

Bit position	Name	Function
0	CF	Carry flag: Set on high-order bit carry or borrow; cleared otherwise
2	PF	Parity flag: Set if low-order 8-bit of result contain an even number of 1-bit; cleared otherwise
4	AF	Set on carry from or borrow to the low-order 4-bits of AL; cleared otherwise

6	ZF	Zero flag: Set if result is zero; cleared otherwise
7	SF	Sign Flag: Set equal to high-order bit of result (0 is positive, 1 if negative)
8	TF	Signal step flag: Once set, a single-step interrupt occurs after the next instruction executes; TF is cleared by the single-step interrupt
9	IF	Interrupt-enable flag: When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location.
10	DF	Direction flag: Causes string instructions to auto decrement the appropriate index register when set; clearing DF causes auto increment.
11	OF	Overflow flag: Set if the signed result cannot be expressed within the number of bits in the destination operand; cleared otherwise.

8086 flags: DF, IF and TF can be set or reset to control
the operations of the processor. The remaining flags are status indicators.